REMARKS

The Office Action of **May 8, 2002** has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One (1) Month Extension of Time* that extends the shortened statutory period for response to **September 8, 2002**. Accordingly, Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-11 were pending the present application prior to the above amendment, with claims 8-11 being withdrawn from consideration. By the above amendment, claims 1, 3-5 and 7 are amended and claim 6 is canceled without prejudice. Accordingly, claims 1-5 and 7-11 remain pending in this application, of which claims 1-5 and 7 are believed to be in condition for allowance for the reasons stated below.

A. Objection to the Specification

The title of the invention is objected to as being non-descriptive. In response thereto, the title of the invention has been replaced with the following title of invention: "HIGH-VOLTAGE MOS TRANSISTOR." Accordingly, withdrawal of the objection is respectfully solicited.

B. Objection to the Drawings

FIGS. 11, 12, 13(a)-13(d), 14(a) and 14(b) are objected to as not being designated as "Prior Art." In response thereto, Applicant files concurrently herewith a *Request for Approval of Drawing Corrections* which properly designates the aforementioned drawing figures as "Prior Art." Accordingly, withdrawal of the objection is respectfully solicited.

C. 35 U.S.C. 112, 1st Paragraph Rejection

Claim 7 stands rejected under 35 U.S.C. §112, 1st paragraph as nonenabling. Applicant respectfully traverses this rejection for at least the following reasons.

It is well established that "claims are not rejected as broader than the enabling disclosure under 35 U.S.C. 112 for non-inclusion of limitations of factors which must be presumed to be within the level of ordinary skill in the art; claims need not recite such factors where one of ordinary skill in the art to whom the specification and claims are directed would consider them obvious." *In re Skrivan*, 427 F.2d 801, 806, 166 USPQ 85, 88 (CCPA 1970).

In the present situation, Applicant contends that the "forward biased breakdown voltage" recited in claim 7 is well known in the art. For instance, the actual characteristic of the relationship between the current and voltage of the PN junction diode is such that the current only starts to flow when a forward bias voltage is applied to the diode and becomes higher than a fixed voltage known as "semi-ideal threshold voltage." Hence, the current does not flow once 0V is exceeded. Insofar as the "forward biased breakdown voltage" of claim 7 corresponds to the aforementioned "semi-ideal threshold voltage," which is well known and easily understood to one having ordinary skill in the art, no issue of non-enablement exists. Accordingly, withdrawal of the rejection is respectfully requested.

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D. 35 U.S.C. 112, 2nd Paragraph Rejection

Claim 4 stands rejected under 35 U.S.C. §112, 2nd paragraph as indefinite. In order to more clearly define the claimed subject matter, claim 4 is amended so that the limitation

"wherein a size of the source offset region is not equal to a size" recites "wherein a length of the source offset region is set longer than a length." Accordingly, withdrawal of the rejection is respectfully requested.

E. 35 U.S.C. 102 Rejection

Claims 1-6 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,084,283 to Arai. Applicant respectfully contends that the claimed subject matter as presently amended clearly defines over Arai for at least the reasons set forth hereinbelow.

1. Summary of the Invention

The claimed invention in accordance with claims 1-6 is directed generally to a high-voltage MOS transistor wherein a resistance value of a source region is set independently of a resistance value of a drain region in such a manner as to maintain a high sustaining breakdown voltage of the transistor.

Hence since a high sustaining breakdown voltage is maintained, even if high voltage for operating the transistor is applied to the drain region, sustaining breakdown (i.e., the phenomenon that occurs due to the PN junction of the source offset region becoming forward bias and the flow of the current increases abruptly, according to the voltage of the source offset region and the voltage of the substrate region directly under the gate insulating film) can be prevented.

2. Arai Fails to Teach the Claimed Invention

Applicant respectfully contends that Arai clearly fails to teach or inherently describe the claimed subject matter set forth in the present invention. For instance, Arai teaches at column 10, lines 46-48, that the resistance value of a source portion (115) is set low such that a parasitic capacitance of source portion (115) can hardly have any influence on a transistor channel current. Hence, Arai fails to teach, disclose or suggest a device in which the resistance value of the source region is set independently of the resistance value of the drain region in such a manner as to maintain a high sustaining breakdown voltage, as presently set forth in claim 1-6.

In accordance with column 10, lines 51-55 of Arai, the breakdown voltage is increased by setting a high resistance value for a drain region (116). However, this is different from the claimed subject matter in that the breakdown voltage in Arai is a voltage which relates to the breakdown of the drain region and is the drain voltage (drain breakdown voltage) of the time when the PN junction breakdown, as an electric field converges between the drain region and the gate lower portion when high voltage is applied to the drain region (see page 1, lines 22-25 of the present specification).

Conversely, the sustaining breakdown voltage of the claimed invention relates to the breakdown voltage of the source region (see page 8, line 8 to page 9, line 10 of the present specification). When high voltage is applied to the drain region, the substrate current increases, which causes the voltage of the substrate region directly under the gate insulating film to change. Thereafter, the PN junction between the substrate directly under the gate insulating film and the source region is forward biased, current flows through the PN junction, and the drain voltage is

generated as the sustaining breakdown voltage. Hence, the sustaining breakdown voltage of the claimed invention is completely different and patentably distinct from the breakdown voltage of Arai.

Thus, insofar as Arai fails to teach the claimed subject matter of the present invention, anticipation of claims 1-6 under §102 cannot be supported. Accordingly, withdrawal of the rejection is earnestly solicited.

F. 35 U.S.C. 103 Rejection

Claims 1, 2 and 7 stand rejected under 35 U.S.C. §103(a) as unpatentable over Prior Art FIG. 13(d) in view of JP 1-305573 to Yoshihisa. Applicant respectfully contends that the proposed combination of references fails to teach, disclose or suggest the claimed subject matter of claims 1, 2 and 7 as presently amended.

1. Summary of the Invention

As previously indicated hereinabove, amended claims 1 and 2 of the claimed invention recites that the source region is set independently of a resistance value of a drain region in such a manner as to maintain a high sustaining breakdown voltage of the transistor based on a voltage of a source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

Further, amended claim 7 recites that the resistance of the source region is set higher than that of the drain region such that (the voltage of the substrate directly under the gate-forward

biased breakdown voltage) does not easily exceed the voltage of the source offset region.

2. The Combination of References Fails to Disclose the Claimed Invention

As expressed in the English Abstract of Yoshihisa, "a drain 1 and a source 2" is disclosed, however, "the source 1 or the drain 2" is disclosed in line 11. Since according to the Japanese Unexamined Patent Publication 1-305573, "1: source, 2: drain," "source 1 and drain 2" is the correct interpretation. Hence, reference numeral (12) of Fig. 1 in Yoshihisa refers to a source offset region and reference numeral (22) refers to a drain offset region.

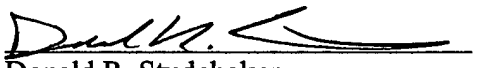
Therefore, in the high breakdown voltage MOS transistor of Yoshihisa, the resistance value of the source offset region is lower than that of the drain offset region. As a result, for such a structure, since the resistance value of the source offset region is low, the voltage of the source offset region will not become high even if current flows through the source offset region during operation of the transistor. Hence, since the voltage of the substrate directly under the gate forward biased breakdown voltage easily exceeds the voltage of the source offset region, the MOS transistor of Yoshihisa cannot have a high sustaining breakdown voltage, which is required by the claimed invention.

In view of the foregoing reasons, the teachings of Yoshihisa, even when combined with the alleged Prior Art disclosure of Fig. 13(d) of the present specification, is completely different from the claimed invention. Thus, a finding of *prima* facie obviousness cannot be supported by their resultant combination. In view of the foregoing remarks, withdrawal of the rejection is respectfully solicited.

Conclusion

Accordingly, Applicant respectfully contends that the claimed invention defines subject matter that is clearly patentably distinct over the prior art of record. It is respectfully requested that the rejection be withdrawn. If the Examiner believes further discussions with Applicants' representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,



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MARKED UP VERSION OF AMENDED CLAIMS

1. (Amended) A high-voltage MOS transistor wherein a resistance value of a source region is set independently of a resistance value of a drain region in such a manner as to [increase a] maintain a high sustaining breakdown voltage of the transistor, which is based on a voltage of a source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

3. (Amended) [A high-voltage MOS transistor comprising:

a drain offset region; and

a source offset region, which is asymmetrical to the drain offset region,

whereby the transistor has a high sustaining breakdown voltage] The transistor of Claim 2, wherein the resistance value of the source offset region is set higher than the resistance value of the drain offset region.

4 (Amended) The transistor of Claim [3] 2, wherein a [size] length of the source offset region is [not equal to a size] set longer than a length of the drain offset region [such that the transistor has the high sustaining breakdown voltage].

5. (Amended) The transistor of Claim [3] 2, wherein a dopant concentration of the source offset region is [not equal to] set lower than a dopant concentration of the drain offset region [such that the transistor has the high sustaining breakdown voltage].

7. (Amended) The transistor of Claim 1, wherein the resistance value of the source region is set higher than that of the drain region such that [a substrate voltage] the voltage of the substrate region directly under the gate insulating film VW minus a forward biased breakdown voltage of silicon does not exceed a source voltage VS easily, during operation of the high-voltage MOS transistor.